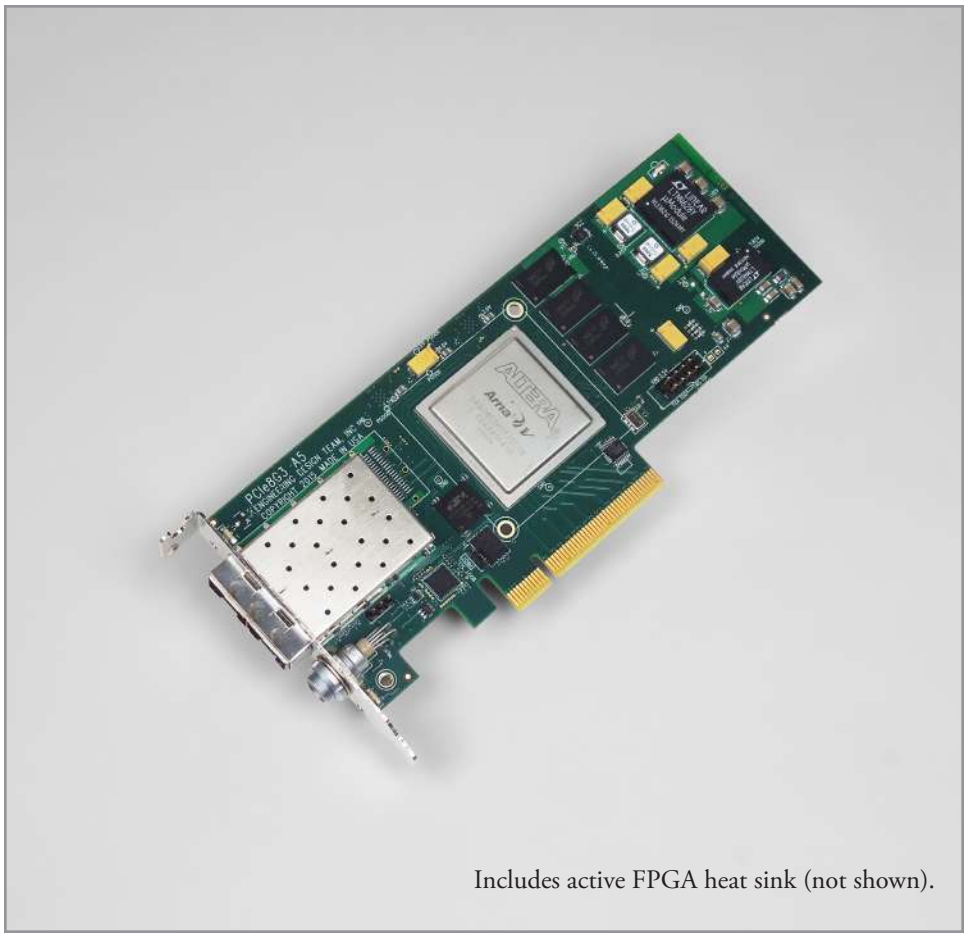
Parhelia B.V.
www.parheliabv.com
+31(0)10 741 00 28

PCIe8g3 A5-10G

PCIe Gen3 x8 board with Arria V FPGA and up to two 10G SFP/+s



Includes active FPGA heat sink (not shown).

Description

The PCIe8g3 A5-10G is a fast, versatile low-profile PCI Express (PCIe, Gen3) x8 interface, available with either a full or a half-height back panel. It has up to two 10G SFP/+ ports and supports 1/10GbE, OC3/12/48/192 (STM1/4/16/64), or OTU1/2/2e/2f.

Each port has its own reference clock, programmable for 1–808 MHz, and links to the FPGA for serialization / deserialization (SERDES) and clock recovery.

The single FPGA is an Altera Arria V GZ (E3, E5, or E7) with access to one 64-bit wide 2 GB block of DRAM (DDR3), which can act as s data buffer. The FPGA provides up to 8 independent DMA channels via EDT FPGA configuration files.

A time code input (1 pps or IRIG-B) also is included, with an option for either DB9 or BNC cabling.

EDT FPGA configuration files are included to support 1GbE and 10GbE (at the PCS and PMA layers); OC3/12/48/192 and OTU1/2/2e/2f (raw, framed, framed and descrambled); and demultiplexing. Custom files can be requested.

Features

- PCIe (Gen3) x8 half-height interface (full- or half-height back panel) with up to two 10G SFP/+s
- Data formats: 1/10GbE, OC3/12/48/192 (STM1/4/16/64), OTU1/2/2e/2f
- FPGA + DMA: One user-programmable Altera Arria V 5AGZ (E3, E5, or E7), configurable for up to 8 independent DMA channels
- DRAM (DDR3): One 64-bit wide block of 2 GB
- EDT intellectual property for 10GbE PCS and PMA layers, SONET/SDH framing, demultiplexing, and G.709 framing
- Time code input: 1 pps or IRIG-B, with user-configurable output

Applications

- Telecommunications monitoring, recording, and processing
- SONET/SDH to ethernet conversion
- Multiple other network processing applications

Specifications

FPGA Resources + DMA	One programmable FPGA, Altera Arria V GZ	E3, E5, or E7, user-configurable for up to 8 independent DMA channels
Memory	DRAM (DDR3), one 64-bit wide 2 GB block for snapshot recording / data buffering	
Clocks (Reference)	Each port (one or two) has a reference clock, independently programmable from 1 to 808 MHz, plus support for reference loop timing.	
Data Rates	Dependent on such factors as data format and system variables.	
Data Format (I/O)	Via multiple ports, the board supports various data formats as shown below: 1/10GbE, OC3/12/48/192 (STM1/4/16/64), OTU1/2/2e/2f). Also provided is a time code input (to connect to an external source) for 1 pps, IRIG-B, or other input, with user-configurable output.	
PCI Express Compliance	PCIe version Number of DMA channels Number of lanes	3.0 8 8
Transceivers	The board has multiple transceiver options, as shown below.	

Up to two SFP/+*	**ELECTRICAL (1GbE) SFP only**	**OPTICAL SFP/+* 1550 nm**	**SFP/+* 1310 nm**	**SFP/+* 850 nm**
Output power (dBm)	–	–2 to +3 / 0 to +4	–9.5 to –3 / –8.2 to +0.5	–9 to –2.5 / –5 to –1
Center wavelength (nm)	–	1500–1580 / 1530–1565	1270–1360 / 1260–1355	830–860 / 840–860
Sensitivity (dBm)	–	–28 / –23	–18 / –10.3	–18 / –7.5
Max input power (dBm)	–	–9 / –7	0 / +0.5	0 / +0.5
Connector	RJ45 transceiver	LC	LC	LC

* An **SFP** at 1550, 1310, or 850 nm can support 1GbE, OC3/12/48 (STM1/4/16), or OTU1.
An **SFP+** at 1550 or 1310 nm can support 10GbE, OC192 (STM64), or OTU2/2e/2f — or, at 850 nm, 10GbE only.

Cooling	Active heat sink	
Connectors	One 7-pin Lemo for time code input One RJ45 or LC on each SFP/+ as shown above	
Cabling	To 7-pin Lemo on board, from time code source For other cabling, consult EDT for purchase options.	Via one DB9 (for 1 pps or IRIG-B) or BNC (for IRIG-B only)
Physical	Weight Dimensions	4.0 oz. (typical, with active heat sink but without transceivers) 6.6 x 2.7 x 0.75 in.
Environmental	Temperature (operating / non-operating) Humidity (operating / non-operating)	0° to 40° C / -40° to 70° C 1% to 90%, non-condensing at 40° C / 95%, non-condensing at 45° C
System and Software	System must have a PCI Express bus (8 or 16 lanes) that is not dedicated to display use only. Software is included for Windows and Linux; for versions, see edt.com.	

Ordering Options

- Backpanel: Full- or half-height
- FPGA: E3 / E5 / E7
- Transceivers: [options above]
- Cabling (for time code input): DB9 / BNC

Bold is default. For more options, see main board detail. **Ask** about custom options.